High-Power Multilevel Step-Up DC/DC Converter for Offshore Wind Energy Systems

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Abstract — This paper presents a multilevel step-up DC/DC converter for DC grid-based offshore wind energy conversion applications. The main features of the proposed multilevel converter are as follows: 1) the voltage stress of the power devices can be lowered, making it suitable for high-voltage applications; 2) the boost inductor can be significantly reduced which leads to the outstanding dynamic performance; and 3) it can reach a high-voltage gain, which is well suited for high-gain applications. The theoretical analysis is carried out for a four-level step-up converter. Therefore, the converter can be extended to any arbitrary number of levels. The proposed four-level converter is verified by a simulation and evaluated to the conventional multilevel DC/DC converter in terms of component stress and power device count. The developed topology has been implemented on a 2-kW prototype converter to confirm its feasibility.

Index Terms — DC grid-based offshore wind energy, high-voltage gain, multilevel step-up converter.

I. INTRODUCTION

With increasing penetration of renewable and decentralized energy generations into power grids, it is expected that the use of medium-voltage DC (MVDC) transmission and high-voltage DC (HVDC) distribution will expand in the near future. The large renewable energy sources, such as offshore wind farms and photovoltaic power plants, operate more efficiently when they are connected to the MVDC and HVDC grids compared to the AC transmission systems [1-3]. One of the key-enabling components for the DC voltage technology is a high-power step-up DC/DC conversion system that is required for the emerging applications, such as large-scale offshore wind energy systems, to interface with high voltage transmission networks [4-9].

In this regard, step-up DC/DC power conversion systems were introduced for future wind farm DC layouts, as shown in Fig. 1 to meet MVDC and HVDC transmission systems. In [6-7], a step-up converter was introduced for the MVDC and HVDC levels using the high breakdown voltage capability of thyristors. Notable feature of this converter is that only one inductor and single capacitor are employed to reach the high-voltage gain and eliminate turnoff losses of minority carrier devices using soft switching technique. However, the converter suffers from high power device conduction losses because a large number of diodes are needed in high-voltage side. Also, utilizing the thyristor technology limits the switching frequency operation of the converter, which results in the bulky passive components and slow dynamic response. Multiple-module two-level boost converters with a single switch were proposed to achieve a high voltage conversion ratio for offshore wind energy applications [4]. Nonetheless, because of a large duty ratio of the main switch to achieve the high-voltage gain, the switching frequency is limited to reduce losses and get enough the turn-off time for the switches. Hence, increasing the size of passive elements, such as boost inductors and filter capacitors, is inevitable due to the low switching frequency. Furthermore, a number of power devices connected in series is required due to the large voltage stress across the main active switches and diodes, which leads to the complex balancing circuit and high conduction loss. Therefore, two-level conventional DC/DC converters are not suitable choice for high-voltage and high-switching frequency operation. The problem of the high-voltage stress on the conventional boost converters has been solved by the multilevel converters using low-voltage-rated devices with higher switching frequency operating at low blocking voltage levels. In contrast to traditional two-level DC/DC converters, multilevel DC/DC converters greatly reduce the boost inductance requirement and also have much lower device voltage rating and fast dynamic response. Among the existing multilevel DC/DC converters, the diode-clamped and capacitor-clamped multilevel converters are two classical multilevel topologies that are the most widely used in the industry applications [11-12]. The generalized multilevel topology represented in [13] is regarded as the most comprehensive and complicated multilevel topology. Both passive devices (diodes and capacitors) and active switches are used as clamping components in this topology. The main drawback of this topology is a large number of active switches and passive devices, which makes it difficult to be commercialized in practical applications. Modular multilevel DC/DC converters based on the modular multilevel inverter were proposed in [14-15]. The inherent operating mechanism among these topologies is to circulate AC currents to achieve energy balance between their modules. The circulating currents lead to the high conduction losses. A bidirectional
modular multilevel DC/DC converter based on a triangular structure was developed in [16] with significant reductions in the input current and output voltage ripples through interleaved operation of the converter. However, each module has a two-level structure with one boost inductor which increases the difficulty of design considerably for high-voltage applications. In [9], a multilevel boost DC/DC converter derived from a double-boost converter was introduced for high-voltage applications [12]. Although the introduced multilevel converter features the low-voltage stress across clamping capacitors in addition to other aforementioned benefits of the multilevel DC/DC converters, the voltage gain is still similar to that of the traditional two-level DC/DC converters.

Motivated by these challenges, this paper proposes a new multilevel step-up DC/DC converter for DC grid-based offshore wind energy applications, as shown in Fig. 1. The proposed multilevel approach requires three power device arms including an active switch arm connected to the DC voltage source in the middle and two top and bottom diode arms. Therefore, the voltage gain is extended and the voltage stress of the power devices and clamping capacitors are reduced compared to the conventional multilevel converter. Furthermore, the size of input inductor is lowered owing to the smaller input current ripple. The proposed approach is compared to the conventional two- and four-level approaches to demonstrate its advantages in high-voltage offshore wind energy conversion applications. A comprehensive collection of experiments are conducted to evaluate the feasibility of the presented topology.

II. PROPOSED MULTILEVEL STEP-UP DC/DC CONFIGURATION

A. General Topology

Fig. 2 shows the generalized multilevel step-up DC/DC converter including three power device arms, where the DC voltage source $V_s$ is connected to the active switch arm in the middle. The clamping capacitors can be separated symmetrically in two top and bottom sides connected to the power devices. The active switch arm in the middle is shared by both the top and bottom clamping capacitors. Therefore, the number of clamping capacitors connected to each active switch is two capacitors. A small output inductor $L_o$ is inserted before the output capacitor $C_o$ to reduce the output current ripple and is beneficial for the transient response. For the proposed multilevel DC/DC converter, the strategy is based on phase-shifted multicarrier modulation. Therefore, a multilevel converter with $m$ voltage levels requires $(m-1)$ triangular carriers. In this method, all the triangular carriers have same frequency and the same peak-to-peak amplitude, but there is a phase shift of $360°/(m-1)$ between any two adjacent carrier waves [17].
B. Proposed Four-Level DC/DC Converter

The proposed four-level DC/DC converter based on the generalized topology in Fig. 2 is depicted in Fig. 3, operating in steady-state and continuous-conduction-mode (CCM). In this section, the general operation of the proposed four-level converter are explained and discussed. The voltages of clamping capacitors ($C_{b1}$, $C_{b2}$) and ($C_{t2}$, $C_{t3}$) are controlled to be $V_{Cto}/3$ and $2V_{Cto}/3$ so that $V_{Cto}$ and $V_{Cbo}$ are equal [9, 18]. The switching modes of four-level converter are shown in Fig. 4. Because the four-level converter has three independent active switches ($S_1$, $S_2$, and $S_3$), it implies eight switching modes, as depicted in Fig. 4. For the proposed four-level topology, the principle of the phase-shifted modulation is considered, where three triangular carriers are required with a 120° phase displacement between any two adjacent carriers. A duty cycle $D$ is defined as the ratio of duration that the active switches conduct over one switching cycle. Using this modulation strategy, the four-level converter represents three operation regions based on $D$, as shown in Table I. The PWM signals and key current waveforms in these regions are shown in Fig. 5.

<table>
<thead>
<tr>
<th>Operation region</th>
<th>No. switching mode</th>
<th>Duty-cycle ($D$)</th>
<th>Voltage $v_p$ limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>6</td>
<td>0&lt;$D$&lt;1/3</td>
<td>$2V_{Cto}$/3-$V_{Cto}$</td>
</tr>
<tr>
<td>II</td>
<td>6</td>
<td>1/3&lt;$D$&lt;2/3</td>
<td>$V_{Cto}$/3-2$V_{Cto}$/3</td>
</tr>
<tr>
<td>III</td>
<td>6</td>
<td>2/3&lt;$D$&lt;1</td>
<td>0-$2V_{Cto}$/3</td>
</tr>
</tbody>
</table>

1) Operating region I (0<$D$<1/3) [Fig. 5(a)]
For the region I, as can be inferred from Fig. 3, the converter operates in a sequence of Fig. 4(a)-(d)-(b)-(d)-(c)-(d)-(a) over one switching time. It can be observed from Fig. 5 that the voltage over active switches $v_p$ is switched between two potentials, $2V_{Cto}$/3 and $V_{Cto}$. For example, when only $S_1$ is turned ON in Mode I, $C_{t1}$ is discharged whereas $C_{t3}$ is charged, making $v_p=2V_{Cto}/3$. While all the active switches are turned OFF (see Fig. 4(d)), the input inductor current passes through the top and bottom diodes, making $v_p=V_{Cbo}$. In similar fashion, when only one active switch is ON, as shown in Fig. 4(a), (b), and (c), $v_p=2V_{Cto}$/3; otherwise $v_p=V_{Cto}$. Therefore, the operation frequency of the voltage $v_p$ and input inductor current $i_L$ is three times the switching frequency. During this operation region, each clamping capacitor $C_{t1}$, $C_{t2}$, $C_{t3}$, and $C_{b2}$, is charged and discharged equally for duration of $D$ over one switching cycle.

2) Operating region II (1/3<$D$<2/3) [Fig. 5(b)]
When the duty cycle $D$ increases and enters the regions of 1/3<$D$<2/3, three previous Mode IV is replaced by three new Modes V, VI, and VII, as shown in Fig. 4(e), (f), and (g), respectively. As a result, the voltage $v_p$ is switched between the potentials: $V_{Cto}$/3 and $2V_{Cto}$/3, as shown in Fig. 5(b). The operating sequence follows Fig. 4(a)-(c)-(b)-(d)-(e)-(f)-(a) over one switching period. In this operation region, each capacitor is charged and discharged at two switching modes.

For instant, when only $S_1$ or $S_3$ and $S_2$ are turned ON, $C_{t1}$ is discharged. The $C_{t1}$ is charged while only $S_2$ or $S_3$ and $S_1$ are ON.

3) Operating region II (2/3<$D$<1) [Fig. 5(c)]
In this operation region, all the active switches are turned ON at the same time over one switching period, as shown in Fig. 4(h). The Modes I, II, and III are substituted by the Mode VIII. Therefore, the voltage $v_p$ introduces two voltage levels: 0 and $V_{Cto}$/3, as shown in Fig. 5(c). The associated operating sequence of this operating region is Fig. 4(h)-(e)-(h)-(g)-(h)-(f)-(h). In this operation region, the clamping capacitors are charged and discharged when only two active switches are ON.

C. Voltage Gain of the Proposed Converter

In order to obtain the voltage gain of the proposed four-level converter, the volt-second balance conditions of the input inductor $L_i$ and output inductor $L_o$ for one third of the switching period are analyzed. Applying the volt-second balance principle to $L_i$ leads to

$$3D \left( V_s - \frac{2}{3} V_{Cto} \right) = 3 \left( \frac{1}{3} - D \right) \left( V_{Cto} - V_s \right) ,$$

(1)

By applying the principle of volt-second balance to $L_o$

$$\frac{4}{3} V_{Cbo} - V_o = 3 \left( \frac{1}{3} - D \right) \left( V_o - V_{Cbo} \right) ,$$

(2)

By inserting (1) into (2), the voltage gain of the proposed converter can be obtained as

$$\frac{V_o}{V_i} = \frac{1+D}{1-D} .$$

(3)

Equation (3) shows that the ideal voltage gain of the proposed multilevel converter is higher than that of the conventional multilevel converter, which is 1/(1-$D$). Fig. 6 shows the voltage gain characteristics of the conventional and proposed boost converter versus duty cycle. For example, for a typical $D=0.75$, the conventional DC/DC converter has an ideal voltage gain of 4 whereas the proposed topology achieves a voltage gain of 7.
Fig. 4. Switching modes of the proposed four-level DC/DC converter. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI. (g) Mode VII. (h) Mode VIII.

Fig. 5. Key current waveforms of the proposed four-level converter. (a) 0<\text{D}<\frac{1}{3}. (b) \frac{1}{3}<\text{D}<\frac{2}{3}. (c) \frac{2}{3}<\text{D}<1.

D. Inductor Current Ripple Characteristic

The current ripple in the input inductor can be calculated during the storage energy stage or transfer energy stage. Therefore, the inductor current ripple can be expressed as a
function of $V_o$, switching frequency $f_s$, and duty cycle $D$ as

$$
\Delta i_{L_i} = \begin{cases}
\frac{V_o}{3L_i f_s} \frac{D(1-3D)}{(1+D)2} & 0 \leq D \leq 1/3 \\
\frac{V_o}{(3D-1)(3D-2)} & 1/3 \leq D \leq 2/3 \\
\frac{9L_i f_s}{V_o} \frac{(1+D)}{(1+D)(3D-2)} & 2/3 \leq D \leq 1
\end{cases} \tag{4}
$$

where $f_s$ is the switching frequency.

Fig. 7 shows comparison of normalized input inductor current ripple for the proposed four-level and conventional four-level converter. The normalization is given by the factor $3L_i f_s / V_o$. The input current has no ripple in some specific points of the duty cycle, such as $D=1/3$ and $2/3$ for both four-level converters. These points are the transitions between the operation regions. For each operation region there is a duty cycle which implies in maximum current ripple of the inductor. It can be seen that proposed four-level has lower maximum current ripple, especially when duty cycle is larger than $2/3$. In the region III ($2/3 < D < 1$), the maximum current ripple can be reduced about 2 times.

### E. Clamping Capacitor Voltage Ripple

The voltage ripple on the capacitors $C_{ib1}$, $C_{ib2}$, $C_{hs1}$, and $C_{hs2}$ is analyzed in this subsection. The voltage ripple on the clamping capacitors can be calculated during the storage energy stage or transfer energy stage. In this analysis, the clamping capacitors are taken to be identical, i.e., $C_{ib1} = C_{ib2}$, $C_{hs1} = C_{hs2} = C$. For the clamping capacitors, the charge time interval is given by $T_s$ and $T_s/3$ for $D < 1/3$ and $1/3 < D < 2/3$, respectively. For $D > 2/3$, the charge time interval is $(1-D)T_s$. Therefore, the clamping capacitor voltage ripple for the proposed four-level converter can be expressed as

$$
\Delta v_c = \begin{cases}
\frac{I_{L_i}D}{(1+D)Cf_s} & 0 < D < 1/3 \\
\frac{I_{L_i}}{3(1+D)Cf_s} & 1/3 < D < 2/3 \\
\frac{I_{L_i}(1-D)}{(1+D)Cf_s} & 2/3 < D < 1
\end{cases} \tag{5}
$$

where $I_{L_i}$ is the average of input inductor current.

Fig. 8 depicts comparison of normalized capacitor voltage ripples for the proposed and conventional four-level converters. The normalization is given by the factor $Cf_s / I_{L_i}$. It is observed that the maximum voltage ripple occurs for the conventional four-level converter in $D = 1/3$ and $2/3$, for all clamping capacitors. In the case of proposed converter, the voltage ripple is reduced for $D > 1/3$. It can be concluded that a smaller capacitor size is required for the proposed converter because the voltage ripple is reduced at least 25%.

### F. Component Stress Analysis and Comparisons

All power devices of the proposed four-level converter sustain the same blocking voltage stress. However, the current stress of the active switches and power diodes are not equal. Table II lists the average voltage and current stresses of power devices and passive components. It should be noted that the clamping capacitors in the top side have identical voltage and current ratings with the counterparts in the bottom side. Although the number of diodes and capacitors are larger compared to the conventional four-level capacitor-clamped converter, the voltage stress of the components is lower than that of the conventional converter for the same output voltage. A low-voltage rating of power devices can simplify implementation by reducing the balancing network.
components used with series-connected devices and has better switching and conduction performance compared to the switches rated on the high blocking voltage. Therefore, the total cost of converter and the chance of switch failure can be lowered. Furthermore, the current rating of power devices is decreased by a factor of 1/(1+D).

### Table II

<table>
<thead>
<tr>
<th>Topology</th>
<th>Proposed converter</th>
<th>Conventional converter</th>
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<tbody>
<tr>
<td>Voltage rating of clamping capacitors</td>
<td>$V_{c_{\text{prop}}}=V_o(1+D)$, $2V_{c_{\text{con}}}$</td>
<td>$2V_o/3$, $V_o/3$</td>
</tr>
<tr>
<td>Voltage rating of power device</td>
<td>$V_o/3(1+D)$</td>
<td>$V_o/3$</td>
</tr>
<tr>
<td>Current rating of active switch</td>
<td>$2D_{\text{Li}}/(1+D)$</td>
<td>$D_{\text{Li}}$</td>
</tr>
<tr>
<td>Current rating of diode</td>
<td>$(1-D)_{\text{Li}}/(1+D)$</td>
<td>$(1-D)_{\text{Li}}$</td>
</tr>
</tbody>
</table>

The total volt-ampere rating (TVAR) of active switches is defined as the product of the average voltage and current ratings of the power device. For the active switches, the TVARs can be obtained as follows

$$\text{TVAR}_{\text{con}-4L} = \frac{3V_o}{1+D}D_{\text{Li}},$$

$$\text{TVAR}_{\text{prop}-4L} = \frac{3V_o}{3(1+D)} \frac{2D_{\text{Li}}}{1+D} = \frac{2D_{\text{Li}}}{(1+D)} = \frac{2V_o}{3(1+D)}.$$  

Since $g = \frac{V_o}{V_i}$ and the output power, $P_o = V_oI_o = V_iI_i$. Therefore, TVARs for active switches can be obtained as follows

$$\text{TVAR}_{\text{con}-4L} = (g-1)P_o,$$

$$\text{TVAR}_{\text{prop}-4L} = \frac{g^2-1}{2g}P_o.$$  

It can be seen from (8) and (9) that the normalized TVAR of active switch is lower for the proposed converter when the voltage gain is increased.

### III. SIMULATION RESULTS AND COMPARISON

A 4 MW wind turbine with an output medium voltage of 3.3 kV is considered as an input source. This voltage will be boosted to 35 kV for an MVDC transmission through a three-phase AC/DC converter and the proposed four-level topology. The proposed converter is designed to be operated in CCM. The input inductance ($L_i$) is chosen according to (5) with the input inductor current ripple of 150 A (15%$I_i$). Also, it should be noted that the output inductor is designed to operate in CCM mode because an opposite energy transmission is not allowed. For this design, the clamping capacitors are selected 100 µF because the voltage ripple of clamping capacitors is around 550 V. The capacitors $C_o$ and $C_{bo}$ are large enough to reduce the output voltage ripple. The simulation results include relevant voltage and current waveforms of the components at steady-state condition. Fig. 9 shows the simulation current waveforms of the input inductor in CCM and active switches from the top to bottom. It can be seen from Fig. 9(b) that the operating frequency of input inductor is equivalently triple the switching frequency. Fig. 10 depicts the simulation voltage waveforms of the clamping capacitors from the top to bottom. The voltages on the clamping capacitors are well balanced and have the ability to maintain charge balances at steady-state conditions. It can be observed that the voltages $V_{C1}$ and $V_{C2}$ are 6.66 and 13.33 kV that are $V_o/5.25$ and $2V_o/5.25$. Therefore, the voltage stress of each power device is 6.66 kV.

![Fig. 9. Simulation current waveforms. (a) Switching patterns. (b) Input inductor current. (c), (d), and (e) Switches currents.](image)

![Fig. 10. Simulation voltage waveforms. (a) Switching patterns. (b) Input current. (c), (d), and (e) Switches currents.](image)

Here, the proposed four-level configuration is evaluated against the conventional two- and four-level converters in terms of the power device count to highlight its advantages for high-voltage applications. Currently, the high-voltage IGBT with maximum blocking voltage rated up to 6.5 kV. The selected high-voltage IGBT and diode are Infineon
FZ250R65KE3 and DD500S65K3, respectively [19]. For all the configurations, the proposed converter, and conventional two- and four-level converters, each switch or diode is comprised of several series and parallel-connected power devices to withstand the rated voltage and current. Fig. 11 shows that the device count in the proposed converters is much smaller than those of conventional four-level and two-level converters. It is because the voltage blocking of active switches is 6.66 kV whereas the active switch of conventional multilevel four-level and two-level converter suffer from the voltage stress of 11.66 and 35 kV, respectively. A smaller device count simplifies implementation by reducing the balancing network components used with series-connected devices in a valve. Fewer snubbers and rate limiters are required as well.

Fig. 11. Power device count comparison.

IV. EXPERIMENTAL RESULTS

A 2-kW laboratory prototype converter was implemented to confirm the theoretical developments of the proposed four-level converter. A Texas Instruments TMS320F28335 is used to run this setup. The circuit component values and their types are listed in Table III. Fig. 12(a) and (b) shows the experimental waveforms of the inductors and switches currents. It can be seen that output inductor and input inductor have same current ripple due to same inductance values. From Fig. 12(a), the operating frequency of input inductor and output inductor is equivalently triple the switching frequency. Furthermore, the volt-second across the inductor is minimized, therefore, having a great potential to reduce the input inductor requirement. The pole voltage of $v_p$ was measured and is shown in Fig. 12(a) which operates in a frequency three times higher than switching frequency. Fig. 12(b) shows switch currents of $S_1$ and $S_3$. It can be seen that the switches have a 120° phase shift because of used three triangular carriers shifted off 120°.

![Fig. 12. Experimental results of the proposed four-level converter operating in nominal condition, 2-kW. (a) Voltage of pole, input and output inductors currents, and collector-emitter voltage of switch $S_2$. (b) Gate-emitter voltages and currents of switches $S_1$ and $S_4$.](image)

<table>
<thead>
<tr>
<th>Table III</th>
<th>PARAMETERS OF EXPERIMENTAL PROTOTYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
<td>Value</td>
</tr>
<tr>
<td>Input and output inductors</td>
<td>50 µH</td>
</tr>
<tr>
<td>Clamping capacitor ($C_{t1}$, $C_{t2}$, $C_{b1}$, $C_{b2}$)</td>
<td>50 µF</td>
</tr>
<tr>
<td>Capacitor ($C_{to}$, $C_{bo}$)</td>
<td>200 µF</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>10 kHz</td>
</tr>
<tr>
<td>Output power</td>
<td>2 kW</td>
</tr>
</tbody>
</table>

Fig. 13 presents the experimental waveforms of the clamping capacitors voltages and output voltage. The voltages on the clamping capacitors are well balanced and have the ability to maintain charge balances at different loads automatically. In addition, it can be seen that the clamping capacitors are charged and discharged with a phase shift with respect to each other due to the modulation strategy. Therefore, the voltage across the active switches and power diodes is clamped with the maximum value of 92 V ($V_{Cto}/3$).

V. CONCLUSIONS

Step-up DC/DC conversion systems are a key component for DC-grid offshore wind energy systems to interface with high-voltage DC power systems. In this paper, a multilevel step-up DC/DC converter was introduced, which significantly reduces the voltage stress of power devices, switching and
conduction losses, and size of input inductor. A four-level topology operating in CCM was analyzed in detail in this paper. In general, an arbitrary number of levels can be obtained using the proposed configuration. The theoretical analysis shows that the proposed converter can achieve higher voltage gain compared to other counterparts. The simulation and experimental results confirm the feasibility of the proposed converter. Conceptual comparisons of the proposed four-level converter to conventional two- and four-level converters show that the proposed approach is superior in terms of device count and device rating. Therefore, it is a good promising alternative to the existing multilevel step-up topologies for high-voltage applications.

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REFERENCES


Fig. 13. Experimental results of the capacitors voltages in nominal condition, 2-kW. (a) Clamping capacitors voltages. (b) Voltages of capacitors C_{bo} and C_{bo}, and output voltage.